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1 Reducing the cost of branches by using registers

Jack W. Davidson, David B. Whalley

May 1990 **ACM SIGARCH Computer Architecture News , Proceedings of the 17th annual international symposium on Computer Architecture**, Volume 18 Issue 3

Full text available: pdf(1.11 MB) Additional Information: full citation, abstract, references, citings, index terms

In an attempt to reduce the number of operand memory references, many RISC machines have thirty-two or more general-purpose registers (e.g., MIPS, ARM, Spectrum, 88K). Without special compiler optimizations, such as inlining or interprocedural register allocation, it is rare that a compiler will use a majority of these registers for a function. This paper explores the possibility of using some of these registers to hold branch target addresses and the corresponding instruction at each branc ...

2 Toward zero-cost branches using instruction registers

Kent D. Wilken, David W. Goodwin

December 1992 **ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture**, Volume 23 Issue 1-2

Full text available: pdf(645.74 KB) Additional Information: full citation, references, citings, index terms

3 Compiler synthesized dynamic branch prediction

Scott Mahlke, Balas Natarajan

December 1996 **Proceedings of the 29th annual ACM/IEEE international symposium on Microarchitecture**

Full text available: pdf(1.50 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Branch prediction is the predominant approach for minimizing the pipeline breaks caused by branch instructions. Traditionally, branch prediction is accomplished in one of two ways, static prediction at compile-time via compiler analysis or dynamic prediction at run-time via special hardware structures. In this paper, we propose a novel technique that aims to combine the strengths of the two approaches -- the lower cost of compile-time analysis with the effectiveness of dynamic prediction. Specif ...

Keywords: branch instruction, compiler analysis, dynamic branch prediction, pipelined processor, profile information

4 Two-level adaptive training branch prediction
Tse-Yu Yeh, Yale N. Patt
September 1991 **Pr ceedings f the 24th annual international symposium on Microarchitecture**
Full text available: pdf(1.13 MB) Additional Information: full citation, references, citings, index terms

5 Alternative implementations of two-level adaptive branch prediction
Tse-Yu Yeh, Yale N. Patt
August 1998 **25 years of the international symposia on Computer architecture (selected papers)**
Full text available: pdf(1.39 MB) Additional Information: full citation, references, index terms

6 Register renaming and dynamic speculation: an alternative approach
Mayan Moudgill, Keshav Pingali, Stamatis Vassiliadis
December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**
Full text available: pdf(1.49 MB) Additional Information: full citation, references, citings

7 MIDEE: smoothing branch and instruction cache miss penalties on deep pipelines
Nathalie Drach, André Seznec
December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**
Full text available: pdf(952.89 KB) Additional Information: full citation, references

8 Alternative implementations of two-level adaptive branch prediction
Tse-Yu Yeh, Yale N. Patt
April 1992 **ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture**, Volume 20 Issue 2
Full text available: pdf(1.29 MB) Additional Information: full citation, abstract, references, citings, index terms

As the issue rate and depth of pipelining of high performance Superscalar processors increase, the importance of an excellent branch predictor becomes more vital to delivering the potential performance of a wide-issue, deep pipelined microarchitecture. We propose a new dynamic branch predictor (Two-Level Adaptive Branch Prediction) that achieves substantially higher accuracy than any other scheme reported in the literature. The mechanism uses two levels of branch history information to make ...

9 Prediction: Improving branch prediction by dynamic dataflow-based identification of correlated branches from a large global history
Renju Thomas, Manoj Franklin, Chris Wilkerson, Jared Stark
June 2003 **Proceedings of the 30th annual international symposium on Computer architecture**
Full text available: pdf(169.91 KB) Additional Information: full citation, abstract, references

Deep pipelines and fast clock rates are necessitating the development of high accuracy, multi-stage branch predictors for future processors. Such a predictor uses a collection of

predictors, each of which provides its predictions at a different stage of the pipeline front-end. A simple 1-cycle latency line predictor provides predictions in the first stage, followed in a couple of stages later by predictions from a more accurate global predictor. Finally, one or two stages later, a highly accurat ...

10 The effect of speculatively updating branch history on branch prediction accuracy, revisited

Eric Hao, Po-Yung Chang, Yale N. Patt

November 1994 **Proceedings of the 27th annual international symposium on Microarchitecture**

Full text available: pdf(521.49 KB) Additional Information: full citation, abstract, references, citings, index terms

Recent research has suggested that the branch history register need not contain the outcomes of the most recent branches in order for the Two-Level Adaptive Branch Predictor to work well. From this result, it is tempting to conclude that the branch history register need not be speculatively updated. This paper revisits this work and explains when the most recent branch outcomes can be omitted without significantly affecting performance. It also explains why this result does not imply that s ...

Keywords: dynamic branch prediction, out-of-order execution, speculative execution, superscalar processors, two-level adaptive branch prediction

11 A comparison of dynamic branch predictors that use two levels of branch history

Tse-Yu Yeh, Yale N. Patt

May 1993 **ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture**, Volume 21 Issue 2

Full text available: pdf(987.31 KB) Additional Information: full citation, abstract, references, citings, index terms

Recent attention to speculative execution as a mechanism for increasing performance of single instruction streams has demanded substantially better branch prediction than what has been previously available. We [1,2] and Pan, So, and Rahmen [4] have both proposed variations of the same aggressive dynamic branch predictor for handling those needs. We call the basic model Two-Level Adaptive Branch Prediction; Pan, So, and Rahmeh call it Correlation Branch Prediction. In this paper, we adopt th ...

12 Reducing branch misprediction penalties via dynamic control independence detection

Yuan Chou, Jason Fung, John Paul Shen

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Full text available: pdf(3.47 MB) Additional Information: full citation, references, citings, index terms

13 Implementation and analysis of path history in dynamic branch prediction schemes

S. Reches, S. Weiss

July 1997 **Proceedings of the 11th international conference on Supercomputing**

Full text available: pdf(954.47 KB) Additional Information: full citation, references, index terms

14 Superscalar architectures: Reducing the complexity of the register file in dynamic superscalar processors

Rajeev Balasubramonian, Sandhya Dwarkadas, David H. Albonesi

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on**

Microarchitecture

Full text available: pdf(1.34 MB) Additional Information: full citation, abstract, references, citings

Dynamic superscalar processors execute multiple instructions out-of-order by looking for independent operations within a large window. The number of physical registers within the processor has a direct impact on the size of this window as most in-flight instructions require a new physical register at dispatch. A large multi-ported register file helps improve the instruction-level parallelism (ILP), but may have a detrimental effect on clock speed, especially in future wire-limited technologies. ...

15 GPMB—software pipelining branch-intensive loops

Zhihong Tang, Gang Chen, Chihong Zhang, Yingwei Zhang, Bogong Su, Stanley Habib

December 1993 **Proceedings of the 26th annual international symposium on Microarchitecture**

Full text available: pdf(906.47 KB) Additional Information: full citation, references, citings

Keywords: branch overlapping, branch-intensive loop-level parallelism, multi-branch switch, processing element

16 Regular contributions: An alternative to branch prediction: pre-computed branches

Lucian N. Vintan, Marius Sbera, Ioan Z. Mihu, Adrian Florea

June 2003 **ACM SIGARCH Computer Architecture News**, Volume 31 Issue 3

Full text available: pdf(985.31 KB) Additional Information: full citation, abstract, references

Through this paper we developed an alternative approach to the present -- day two level dynamic branch prediction structures. Instead of predicting branches based on history information, we propose to pre - calculate the branch outcome. A pre - calculated branch prediction (PCB) determines the outcome of a branch as soon as all of the branch's operands are known. The instruction that produced the last branch's operand will trigger a supplementary branch condition estimation and, after this opera ...

Keywords: complexity evaluations, dynamic branch prediction, execution driven simulation, multiple instruction issue, performance, pipelining, speculative execution

17 A fine-grained MIMD architecture based upon register channels

Rajiv Gupta

November 1990 **Proceedings of the 23rd annual workshop and symposium on Microprogramming and microarchitecture**

Full text available: pdf(1.01 MB) Additional Information: full citation, abstract, references, citings

This paper discusses the use of shared register channels as a data exchange mechanism among processors in a fine-grained MIMD system with a load/store architecture. A register channel is provided with a synchronization bit that is used to ensure that a processor succeeds in reading a channel only after a value has been written to the channel. The instructions supported by this load/store architecture allow both registers and register channels to be used as operand sources and result destina ...

Keywords: aliasing, channels, fine-grained parallelism, instruction scheduling, multiprocessor system, parallelizing compilers

18 The effect of employing advanced branching mechanisms in superscalar processors

Yen-Jen Oyang, Chun-Hung Wen, Yu-Fen Chen, Shu-May Lin

December 1990 **ACM SIGARCH Computer Architecture News**, Volume 18 Issue 4

Full text available: pdf(689.37 KB) Additional Information: full citation, abstract, index terms

This paper discusses the effect of employing advanced branching mechanisms in superscalar processors. The motivation behind employing advanced branching mechanisms in superscalar processors is to reduce the control dependence, or in other words the number of branch operations, in the program so that instruction-level parallelism can be exploited more effectively. The second effect achieved by reducing the control dependence in the program is a decrease of the amount of branch penalty due to less ...

19 Optimizing delayed branches

Thomas R. Gross, John L. Hennessy

October 1982 **Proceedings of the 15th annual workshop on Microprogramming**

Full text available: pdf(583.38 KB) Additional Information: full citation, abstract, references, citings, index terms

Delayed branches are commonly found in micro-architectures. A compiler or assembler can exploit delayed branches. This is achieved by moving code from one of several points to the positions following the branch instruction. We present several strategies for moving code to utilize the branch delay, and discuss the requirements and benefits of these strategies. An algorithm for processing branch delays has been implemented and we give empirical results. The performance data show that a reason ...

20 Index Register Allocation

L. P. Horwitz, R. M. Karp, R. E. Miller, S. Winograd

January 1966 **Journal of the ACM (JACM)**, Volume 13 Issue 1

Full text available: pdf(1.21 MB) Additional Information: full citation, abstract, references, citings, index terms

A procedure for index register allocation is described. The rules of this procedure are shown to yield an optimal allocation for "straight line" programs.

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Lamar Young, Jr.; Goodman, J.;
Acoustics, Speech, and Signal Processing, IEEE International Conference on IC/ '77. , Volume: 2 , May 1977
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Yang, H.; Elenius, P.; Barrett, S.; Schneider, C.; Leal, J.; Moraca, R.; Moody, R Young-Do Kweon; Deok Hoon Kim; Patterson, D.; Goodman, T.;
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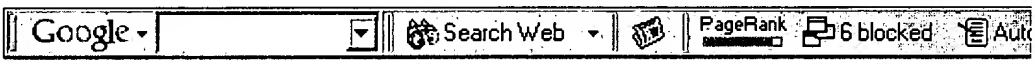
Get the Google Toolbar: 

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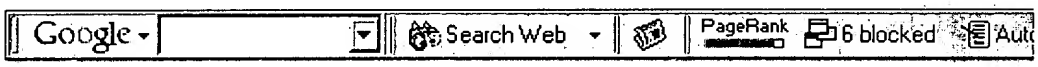
Get the Google Toolbar: 

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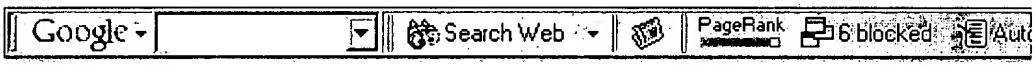
Get the Google Toolbar: 

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